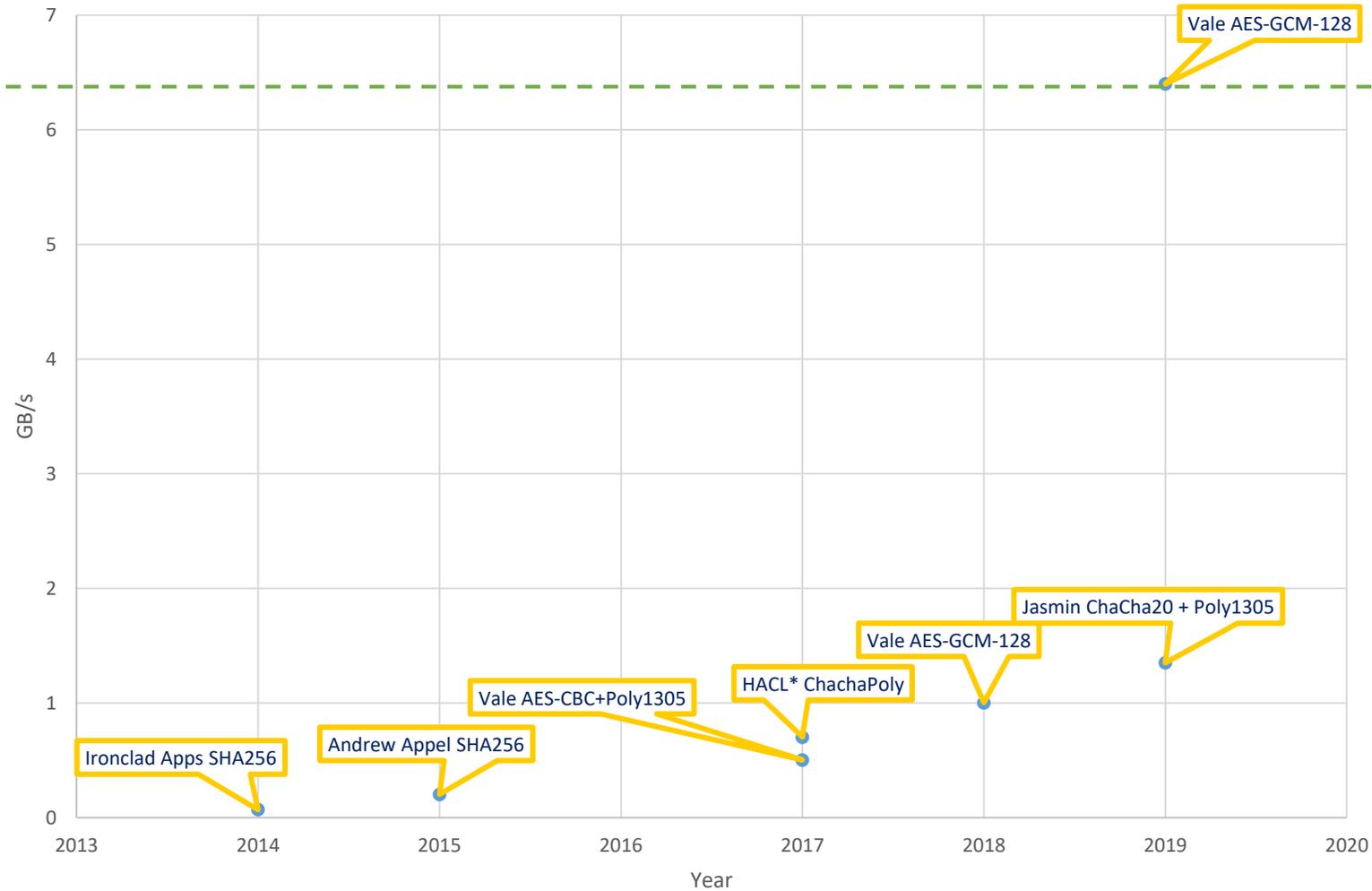


Verified Assembly Language
in Vale / F*

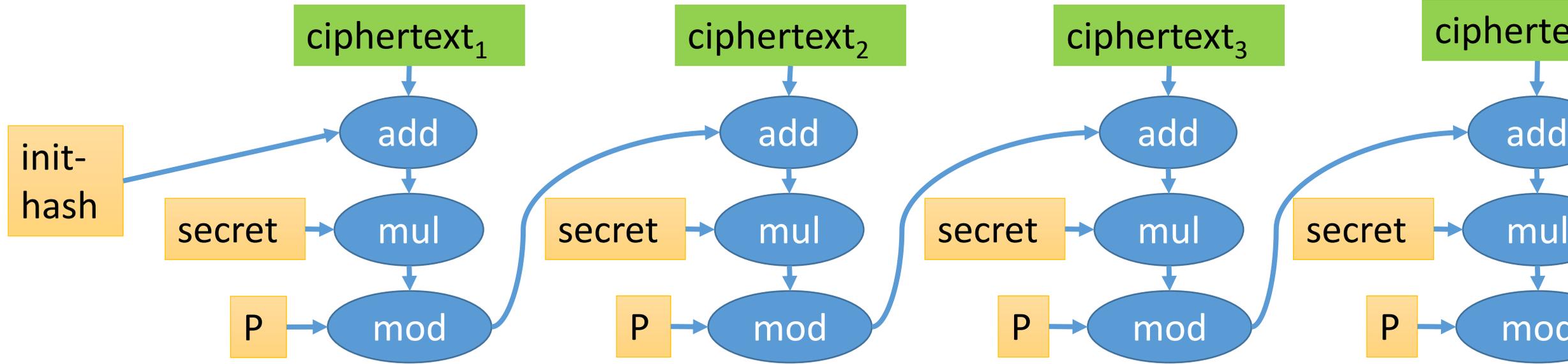
We have a *fast* verified AES-GCM

Performance of various verified symmetric crypto / hash implementations



Fastest
OpenSSL
assembly
code

Optimizing AES-GCM



Important optimizations:

- delay mod operations
- parallelize add/mul operations
- math+bitwise tricks for mod
- careful instruction scheduling

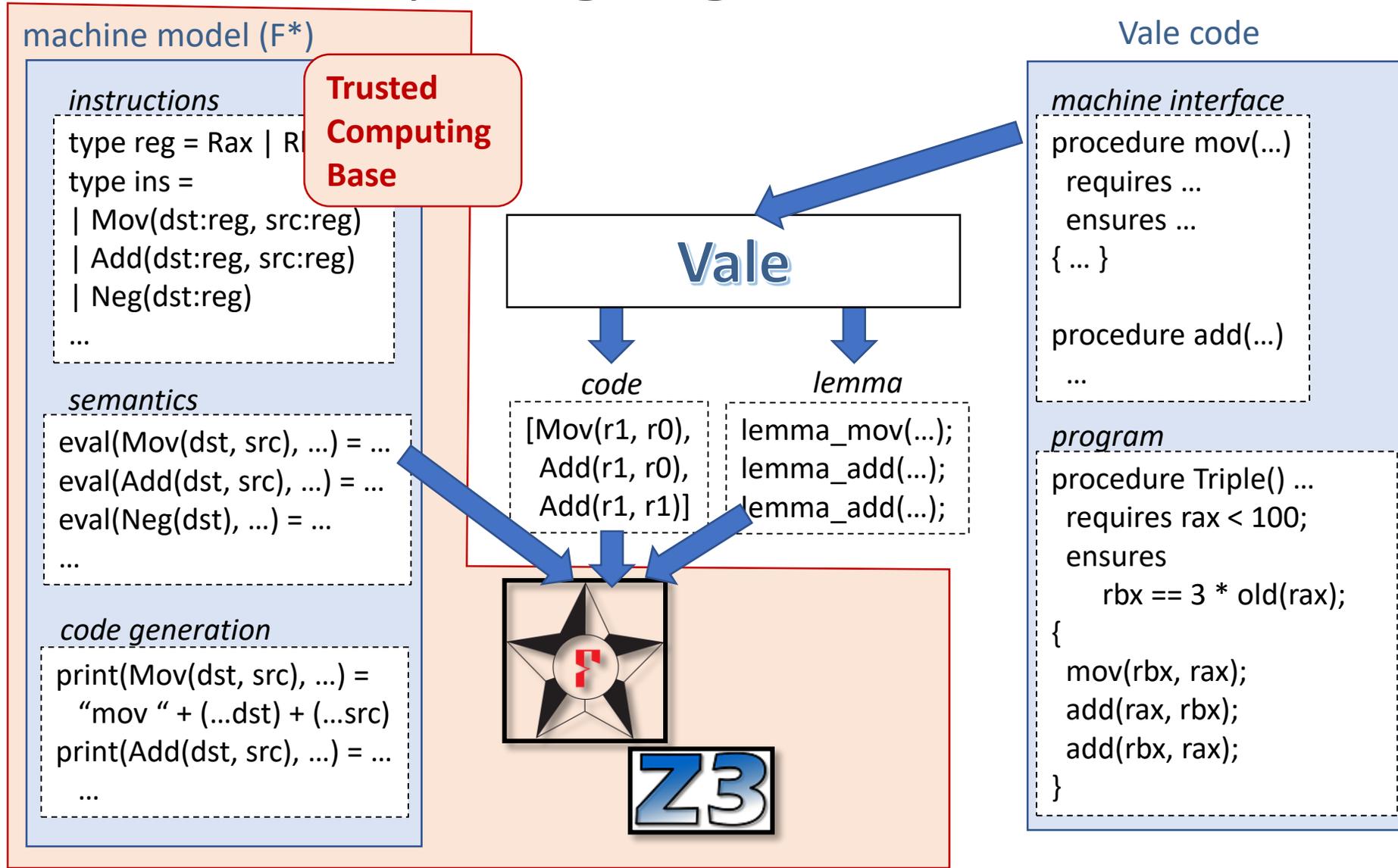
$$(((\text{init} + c_1) * s \% P + c_2) * s \% P + c_3) * s \% P$$

$$\rightarrow (((\text{init} + c_1) * s + c_2) * s + c_3) * s \% P$$

$$\rightarrow ((\text{init} + c_1) * s^3 + c_2 * s^2 + c_3 * s^1) \% P$$

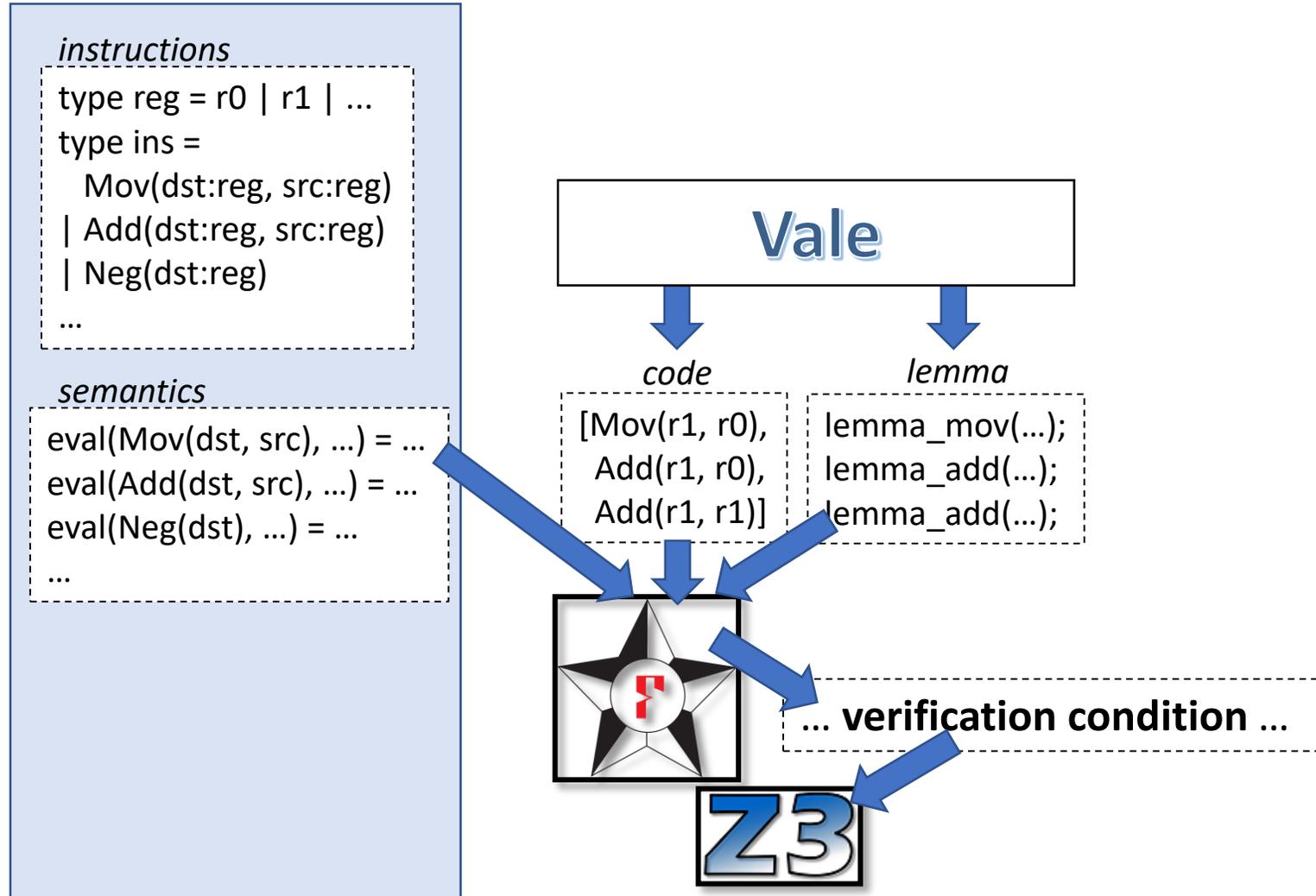
$$\rightarrow ((\text{init} + c_1) * (s^3 \% P) + c_2 * (s^2 \% P) + c_3 * s^1) \% P$$

Vale: extensible, automated assembly language verification



Vale: extensible, automated assembly language verification

machine model (F*)



Verification condition



```
procedure Triple()
  requires rax < 100;
  ensures
    rbx == 3 * rax;
{
1  Move(rbx, rax); // --> rbx1
2  Add(rax, rbx);  // --> rax2
3  Add(rbx, rax);  // --> rbx3
}
```

verification condition

$rax_0 < 100$
|-
($rbx_1 == rax_0 ==>$
 $rax_0 + rbx_1 < 2^{64} \wedge (rax_2 == rax_0 + rbx_1 ==>$
 $rbx_1 + rax_2 < 2^{64} \wedge (rbx_3 == rbx_1 + rax_2 ==>$
 $rbx_3 == 3 * rax_0)))$



Ugh! Default SMT query looks awful!

verification condition we want:

```
..... (rax2 == rax0 + rbx1 ==>
rbx1 + rax2 < 264 .....
```

verification condition we get:

```
...
(forall (ghost_result_0:(state * fuel)).
  (let (s3, fc3) = ghost_result_0 in
    eval_code (Ins (Add64 (OReg (Rax)) (OReg (Rbx)))) fc3 s2 == Some s3 /\
    eval_operand (OReg Rax) s3 == eval_operand (OReg Rax) s2 + eval_operand (OReg Rbx) s2 /\
    s3 == update_state (OReg Rax).r s3 s2) ==>
  lemma_Add s2 (OReg Rax) (OReg Rbx) == ghost_result_0 ==>
  (forall (s3:state) (fc3:fuel). lemma_Add s2 (OReg Rax) (OReg Rbx) == Mktuple2 s3 fc3 ==>
    Cons? codes_Triple.tl /\
    (forall (any_result0:list code). codes_Triple.tl == any_result0 ==>
      (forall (any_result1:list code). codes_Triple.tl.tl == any_result1 ==>
        OReg? (OReg Rbx) /\ eval_operand (OReg Rbx) s3 + eval_operand (OReg Rax) s3 < 264
      )
    )
  )
...

```

Let's write our own VC generator!

- ??? Maybe like this: ???

I'm lonely
and sad.



Our own Vale
VC generator

procedure Triple() ...
...

verification condition we want:

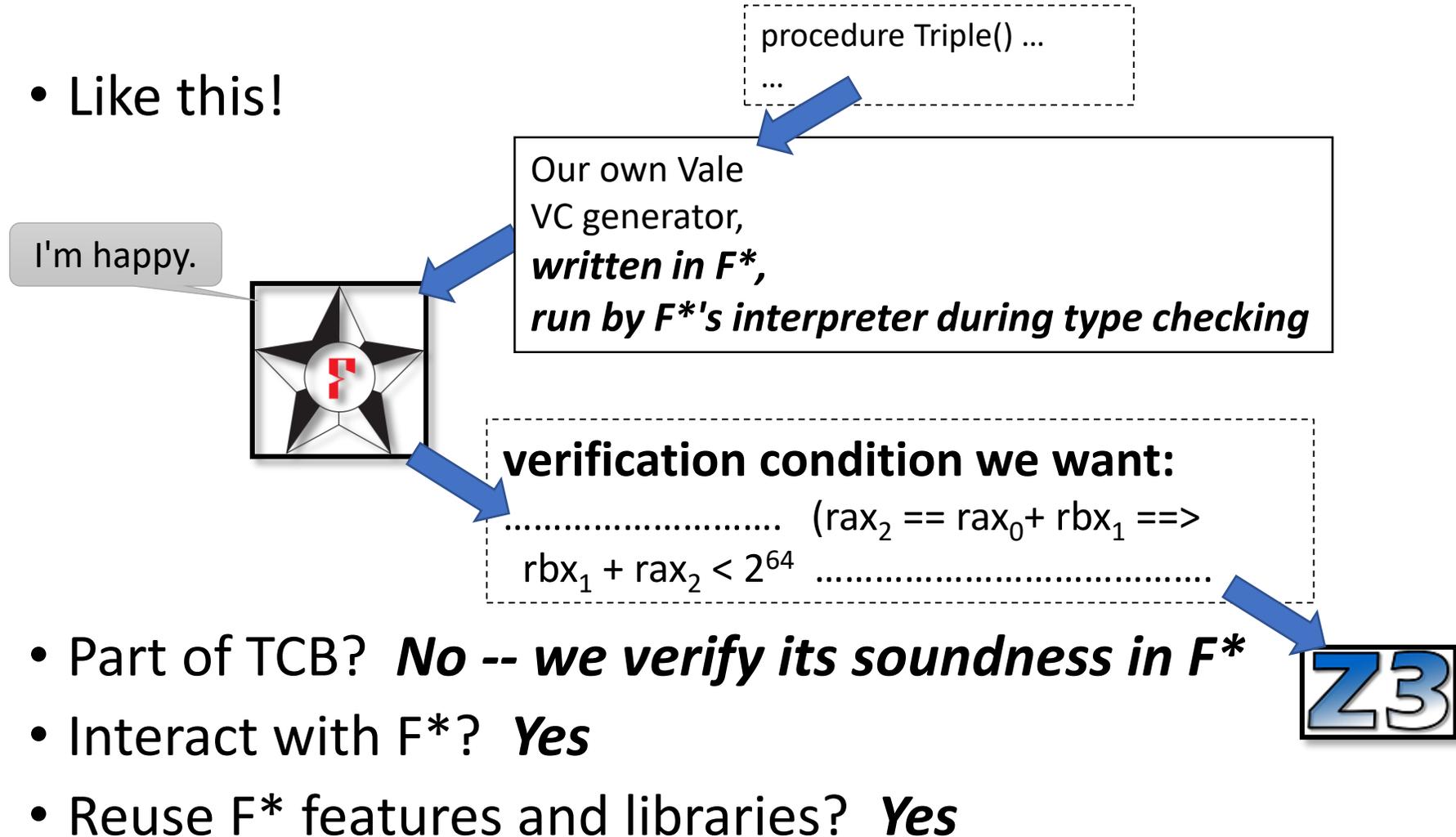
..... (rax₂ == rax₀ + rbx₁ ==>
rbx₁ + rax₂ < 2⁶⁴



- But won't it be part of TCB?
- And how do we interact with F*?
- Can we reuse F* features and libraries?

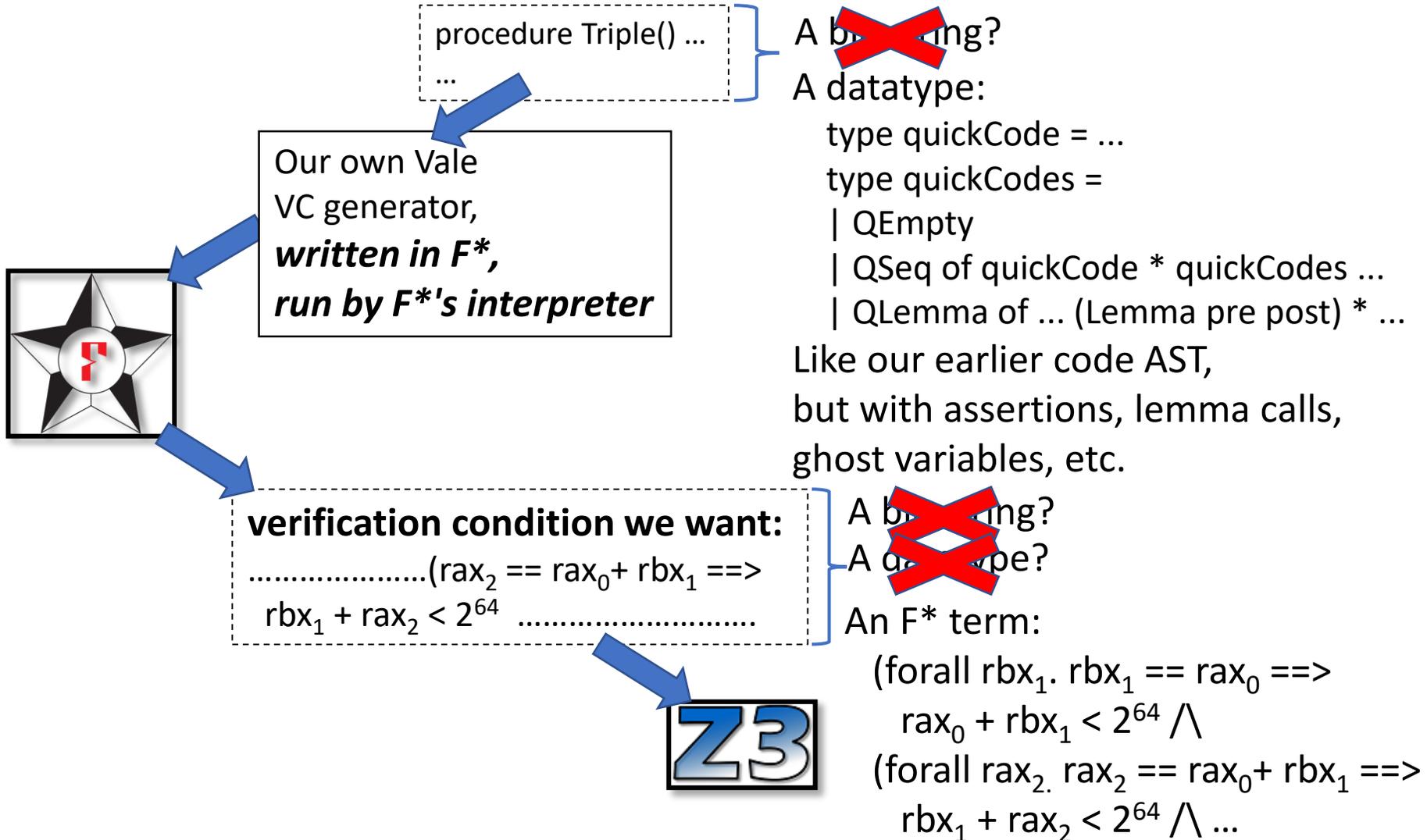
Let's write our own VC generator!

- Like this!



- Part of TCB? **No -- we verify its soundness in F***
- Interact with F*? **Yes**
- Reuse F* features and libraries? **Yes**

Let's write our own VC generator!



Demo

- Verification condition generation for Vale